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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	James E. Jaussi *et al.*	Examiner:	Kenneth Wells
Serial No.:	09/0893,184	Group Art Unit:	2816
Filed:	June 27, 2001	Docket:	884.511US1
Assignee:	Intel Corporation	Customer No.:	21186
Title:	DUAL-STAGE COMPARATOR UNIT		

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on November 4, 2003, from the final rejection of claims 1-9 and 35-43 of the above identified application, as set forth in the final Office action mailed on June 04, 2003.

This Appeal Brief is filed in triplicate and accompanied by authorization to deduct the requisite fee set forth in 37 C.F.R. § 1.17(c).

Real Party in Interest

The real party in interest of the above identified application is the Intel Corporation as identified in the assignment recorded on March 12, 2002 (Reel/Frame 011951/0385) (3 pages).

05/10/2004 AWONDAF1 00000062 190743 09893184
01 FC:1402 330.00 DA

Related Appeals and Interferences

There are no appeals or interferences known to appellants, the appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the decision of the Board of Patent Appeals and Interferences in the pending appeal.

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Status of Claims

Claims 1-9 and 35-43 are currently pending and appealed.

Status of Amendments

No amendments were proposed after the final Office action (mailed on April 11, 2003).

Summary of Invention

A comparator unit includes a first amplifier stage and a second amplifier stage. The first amplifier stage includes a differential amplifier having a pair of input nodes and a pair of output nodes. A switch is connected across the pair of output nodes. A non-linear load is connected across the pair of output nodes. The second amplifier stage is coupled to the pair of output nodes. The second amplifier stage includes an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors. Each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

Issues

Whether the patent office erred in rejecting claims 1-9 and 35-43 as being unpatentable over Nishimura *et al.* (U.S. Patent No. 6,344,761) under 35 U.S.C. § 103(a).

Grouping of Claims

Claims 1-7 and 35-41 stand together for purposes of this appeal. Claims 8-9 and 42-43 stand together for purposes of this appeal.

Argument

Rejections Under 35 U.S.C. 103(a)

Claims 1 and 35 recite, "a switch connected across the pair of output nodes." Claims 2-9 are dependent on claim 1. Claims 36-42 are dependent on claim 35. Claims 8 and 42 recite, "wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes." The final Office action (mailed June 4, 2003) on page 2, at paragraph 3, states:

> Not disclosed is the recited "switch" (line 3 of claim 1) but such would have been obvious to those having ordinary skill in the art because such switches are old and well-known in the art for the well-known purpose of equalizing the output nodes of a differential amplifier prior to comparing the potential difference across the output nodes. The same is true for the limitation of a second switch across the output nodes of the second stage.

Thus, the recited "switch" of independent claims 1 and 35 is not disclosed. In addition, the recited "switch" of dependent claims 8 and 42, referred to as "a second switch" in the Office action, is also not disclosed. A *prima facie* case of obvious requires that the applied references "teach or suggest" each of the claimed elements. *In re Deuel*, 51 F.3d 1552, 1560 (Fed. Cir. 1995). The final Office action applies only Nishimura *et al.* (U.S. Patent No. 6,344,761). However, Nishimura *et al.* fails to disclose the "switch" of claims 1 and 35, the "switch" of claims 8 and 42, and the combination of the "switch" of claims 1 and 35 with the "switch" of claims 8 and 42. Thus, Nishimura *et al.* fails to "teach or suggest" each of the elements of the claims 1-9 and claims 35-43. Therefore, the final Office action fails to state a *prima facie* case of obviousness with respect to claims 1-9 and 35-43.

The Examiner in the final Office action attempts to establish the missing elements through the assertion of Official Notice (traversed in the response filed October 6, 2003) through the common knowledge of a person of ordinary skill in the art. The assertion of Official Notice to establish the missing elements in a 103(a) obviousness rejection on these facts is improper. *In re Sang Su Lee*, 277 F.3d 1338, 1341 (Fed. Cir. 2002), holds

that a conclusion of obviousness "from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference" is an abuse of discretion. The final Office action does not provide a reference to support the assertion that "a switch connected across the pair of output nodes" is well known in the art. Thus, the Office action applies the reasoning of the United States Board of Patent Appeals and Interferences (Board) rejected by the United States Court of Appeals for the Federal Circuit (CAFC) in *In re Sang Su Lee*.

The final Office action also fails to provide a reference to support the assertion that "such switches . . . are . . . well-known for the purpose of equalizing the output nodes of a differential amplifier prior to comparing the potential difference across the output nodes." Again, the Office action applies the reasoning of the Board rejected by the CAFC in *In re Sang Su Lee*.

Further, the final Office action fails to provide a reference to support the assertion that "the limitation of a second switch across the output nodes of the second stage" is also well known in the art. Again, the Office action applies the reasoning of the Board rejected by the CAFC in *In re Sang Su Lee*.

Finally, the Office action fails to provide a reference to support the assertion that the combination of the "switch connected across the pair of output nodes" recited in independent claims 1 and 35 and the "switch connected across the pair of second stage output nodes" recited in dependent claims 8 and 42 is well known in the art. And again, the Office action applies the reasoning of the Board rejected by the CAFC in *In re Sang Su Lee*.

Thus, the rejection of claims 1-9 and 35-43 in the final Office action is an abuse of discretion and therefore improper.

Summary

For the reasons stated above, Appellant respectfully requests withdrawal of the rejections, reconsideration, and allowance of claims 1-9 and 35-43.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief-Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 4th day of May, 2004.

DANNY PADYS _____

Name Signature

Appendix

1. A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage coupled to the pair of output nodes, the second amplifier stage including an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors, wherein each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

2. The comparator unit of claim 1, wherein the differential amplifier comprises a pair of differential pairs of isolated gate field-effect transistors.

3. The comparator unit of claim 2, wherein the switch comprises an electronically controllable switch.

4. The comparator unit of claim 3, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

5. The comparator unit of claim 4, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.

6. The comparator unit of claim 5, wherein each transistor in the pair of cross-coupled isolated gate field-effect transistors comprises an n-channel isolated gate field-effect transistor.

7. The comparator unit of claim 1, wherein the second amplifier stage comprises a non-linear amplifier.

8. The comparator unit of claim 7, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

9. The comparator unit of claim 1, wherein the differential amplifier comprises a differential pair of isolated gate field-effect transistors.

35. A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage including an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors, the input pair of isolated gate field-effect transistors having a pair of gates, wherein the pair of gates are coupled to the pair of output nodes and each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

36. The comparator unit of claim 35, wherein the differential amplifier comprises a pair of differential pairs of isolated gate field-effect transistors.

37. The comparator unit of claim 36, wherein the switch comprises an electronically controllable switch.

38. The comparator unit of claim 37, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

39. The comparator unit of claim 38, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.

40. The comparator unit of claim 39, wherein each transistor in the pair of cross-coupled isolated gate field-effect transistors comprises an n-channel isolated gate field-effect transistor.

41. The comparator unit of claim 35, wherein the second amplifier stage comprises a non-linear amplifier.

42. The comparator unit of claim 41, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

43. The comparator unit of claim 35, wherein the differential amplifier comprises a differential pair of isolated gate field-effect transistors.